

Revision History

0.1 - Initial pre-release
0.2 - Checked by DAB, FJ, JG. Fixed minor mistakes.
0.3 - Removed optic fiber components due to lack of space on the board, added UMAC variant to build list, filled in refdes for build variants

1.0 - Board rev 1. Includes microwave switch assembly components, DAC SHDN pin tied to +5V instead of GND

Build Variants

UMAC chassis compatible

NOUMAC - No UMAC compatibility

Do not populate:
P1

UMAC - Draw power from UMAC

Do not populate:
FL1, F13, D28, U27, C46

Parallel I/O

NOPAR - No Parallel I/O

Do not populate:
U18-21, C39-42, J13, J14

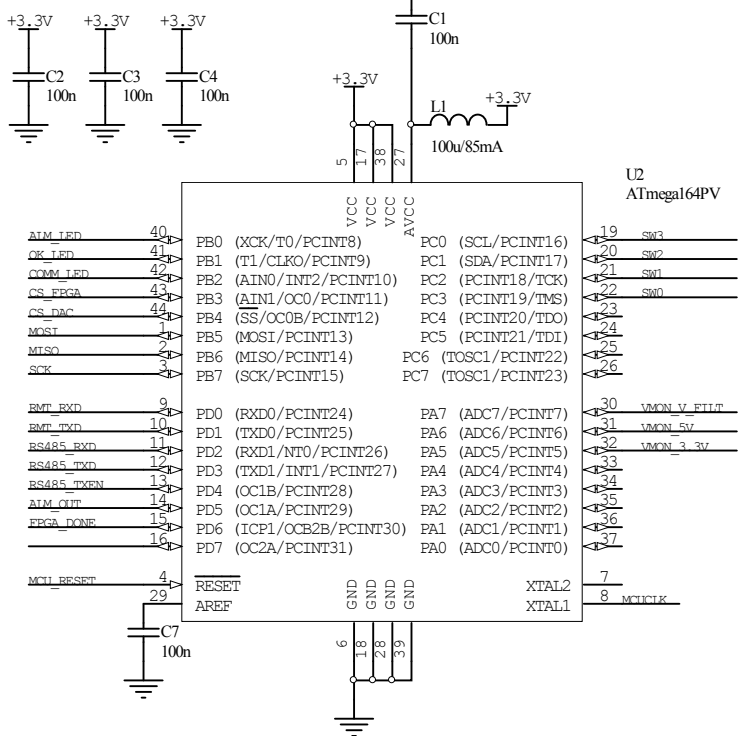
PARIO - With Parallel I/O

Do not populate:

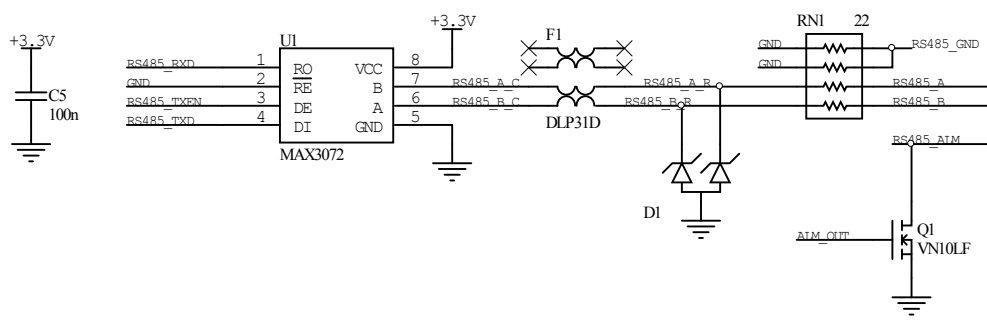
The default configuration is
NOUMAC,
NOPAR

Title <i>Pedestal Interface - Revision History</i>			CSU-CHILL 30750 Weld County Road 45 Greeley, CO 80631	Engineer: JG
Size: Letter	Number: wibeX_pi_1	Revision: 1.0	Colorado State University	Drawn By: JG
Date: 3/24/2009	Time: 2:11:25 PM	Sheet 1 of 8		
File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconvert\ac_revision.SchDoc				

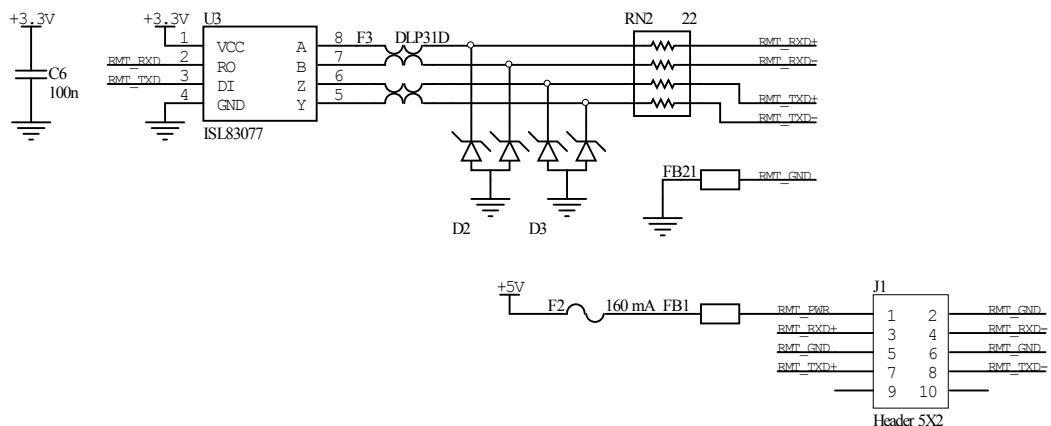
Microcontroller



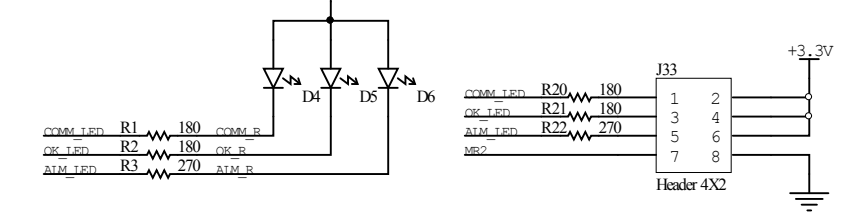
RS485 transceiver, line conditioner



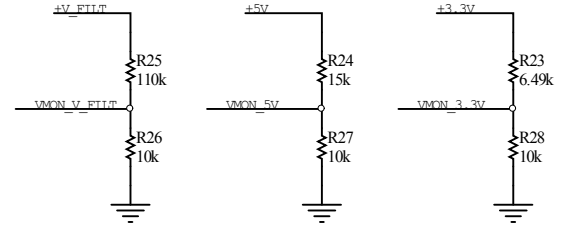
Remote Controller Link



Indicator LEDs

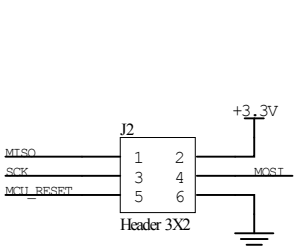


Voltage Monitor dividers

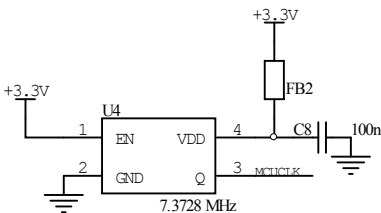


Resistor selection:
 $5k * V_{in} - 10k$
 For 3.3V, 6.5k
 For 5V, 15k
 For 15V, 65k
 For 24V, 110k
 Nominal ADC voltage: 2V

Prog. Connector

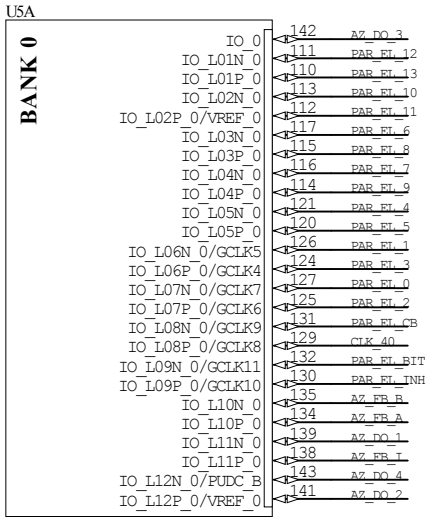


MCU Clock

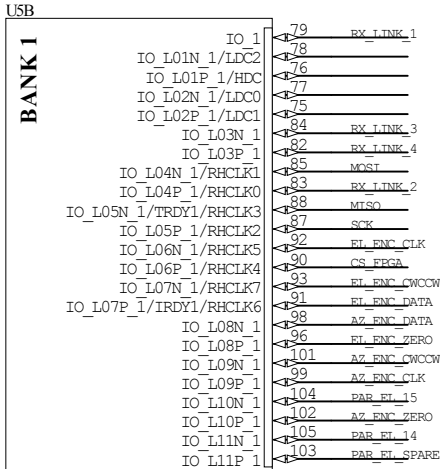


Title Pedestal Interface - Microcontroller			CSU-CHILL 30750 Weld County Road 45 Greeley, CO 80631	Engineer: JG
Size: Letter	Number: wibex_pi_2	Revision: 1.0	Drawn By: JG	
Date: 3/24/2009	Time: 2:11:25 PM	Sheet 2 of 8	Colorado State University	
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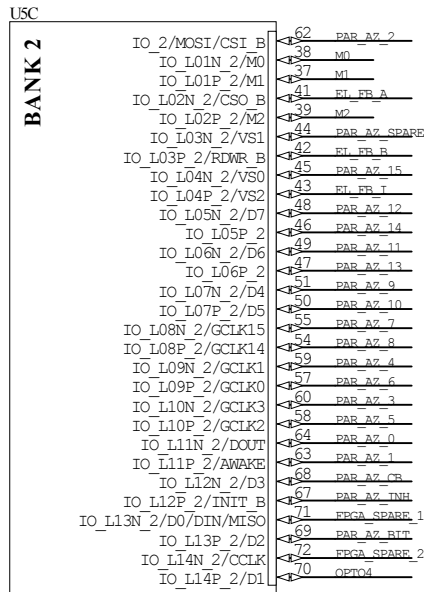
FPGA I/O



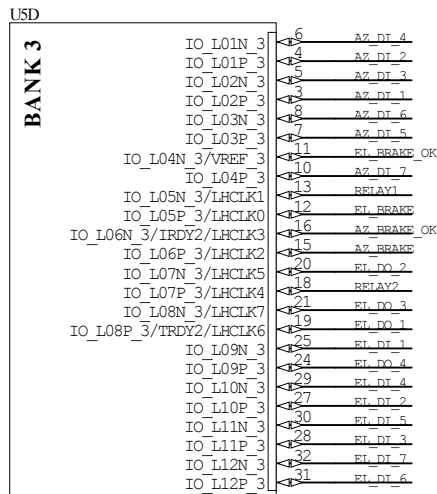
XC3S50AN-4TQ144I



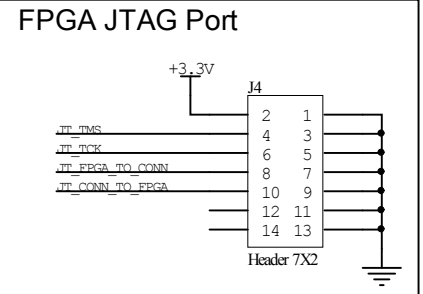
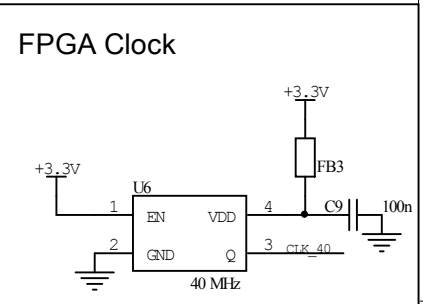
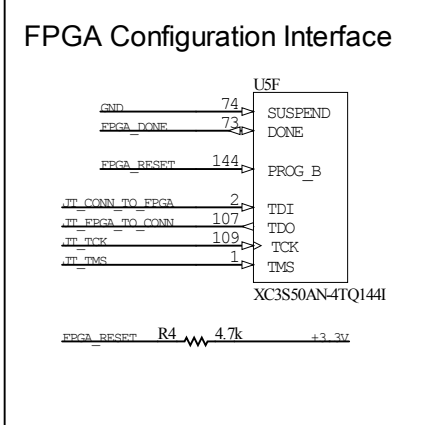
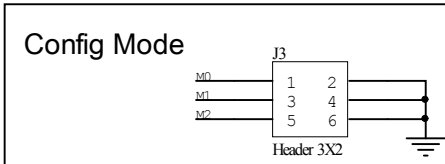
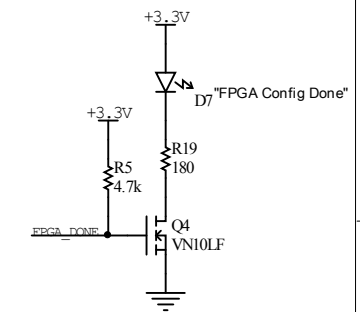
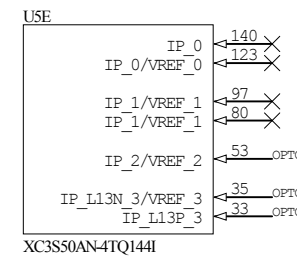
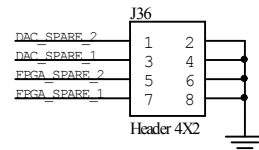
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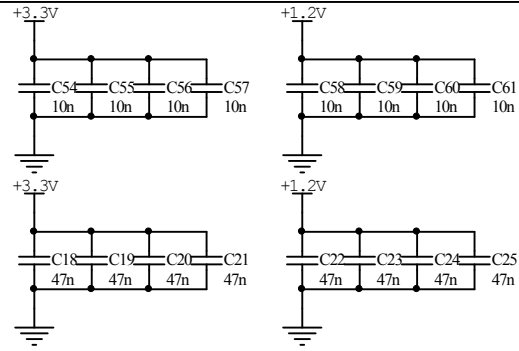
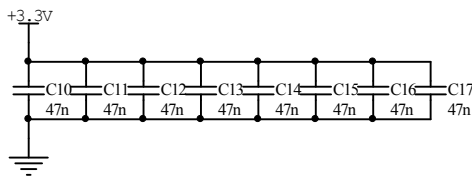
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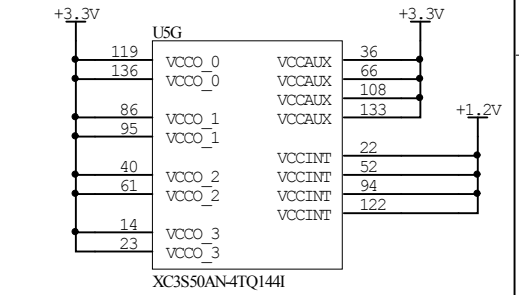
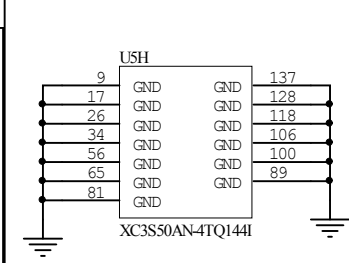
XC3S50AN-4TQ144I



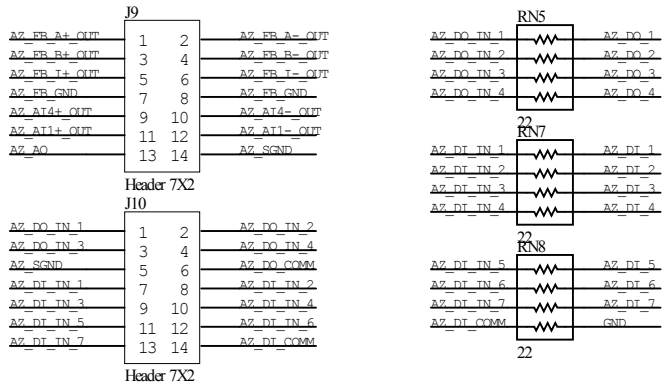
FPGA Supply bypass



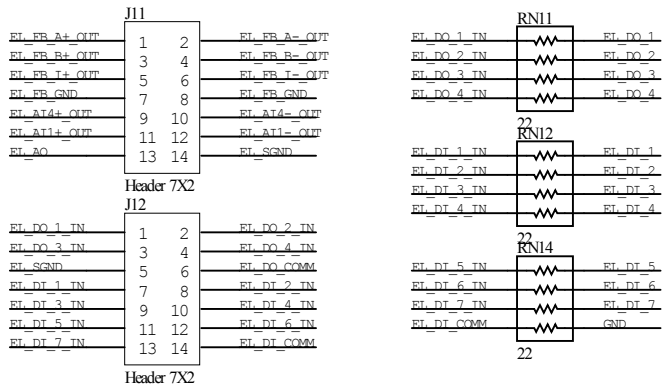
FPGA Power Supply



Azimuth Digital I/O Connector



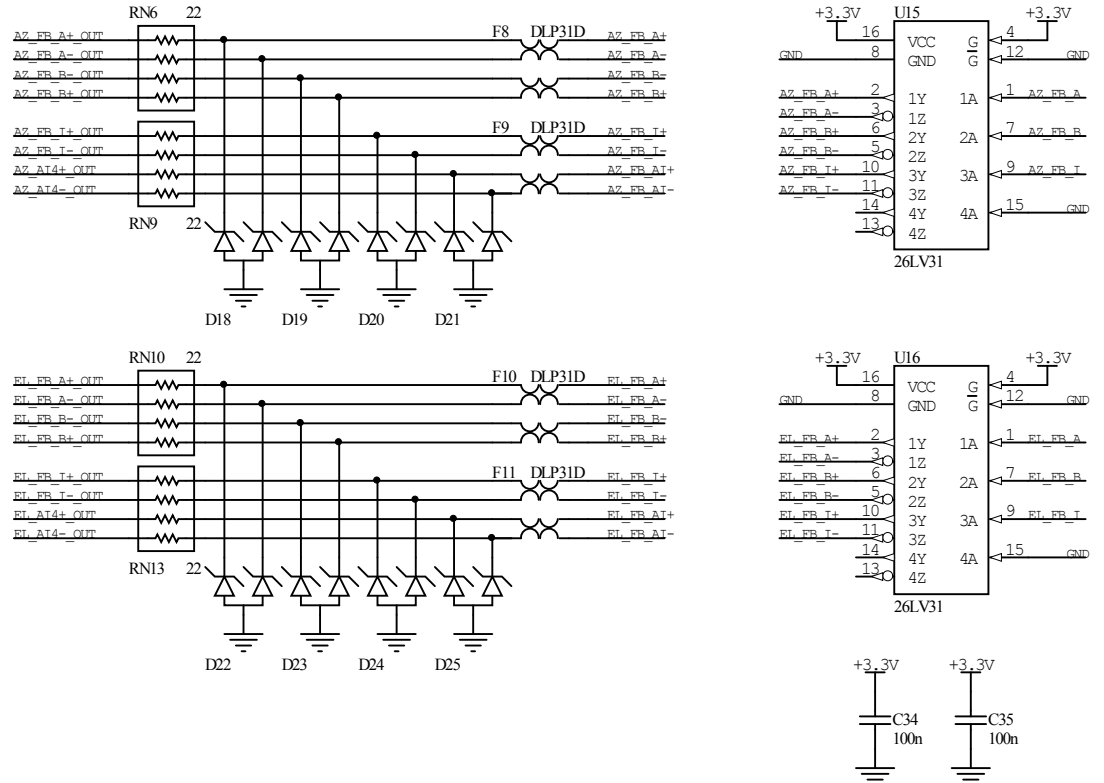
Elevation Digital I/O Connector



Digital I/O Grounding



Simulated Incremental Encoder output drivers, protection network



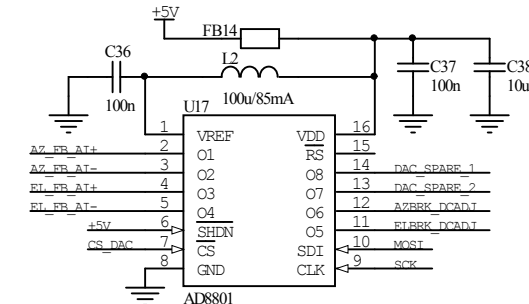
Digital I/O Grounding



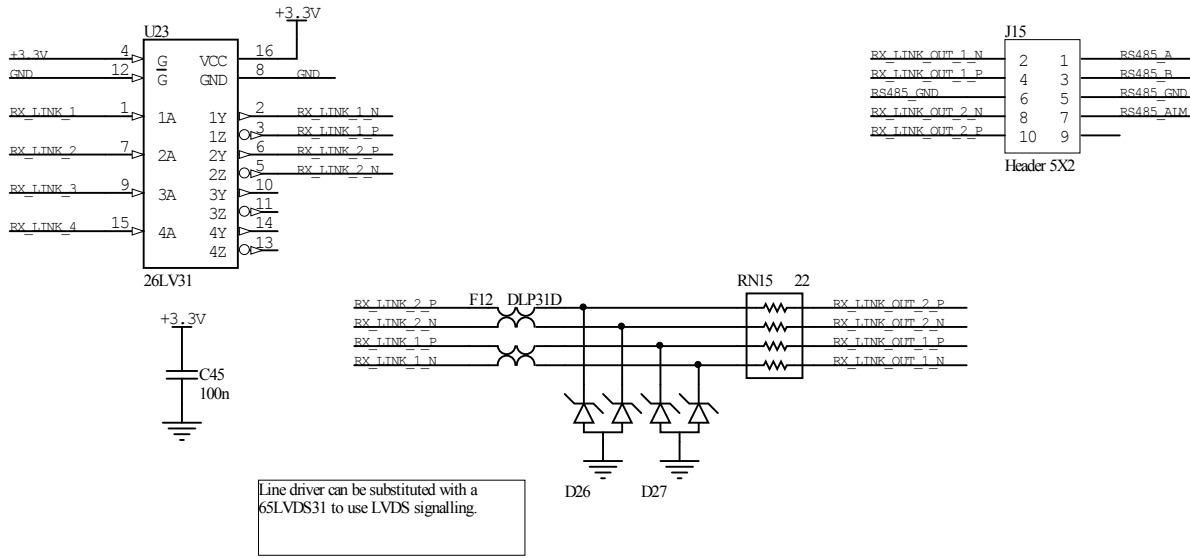
DAC

The DAC controls the Az and EI Analog Inputs differentially (software writes different values to each channel pair)

Also, the duty cycle control for the brake drivers are controlled by output channels 5 and 6



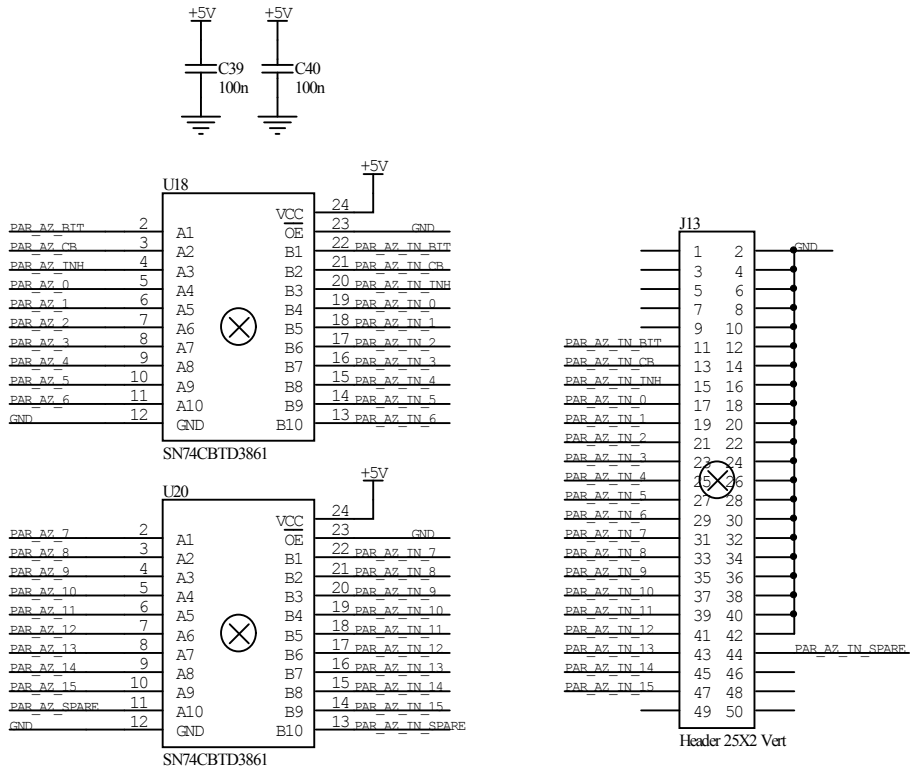
Digital Receiver Link



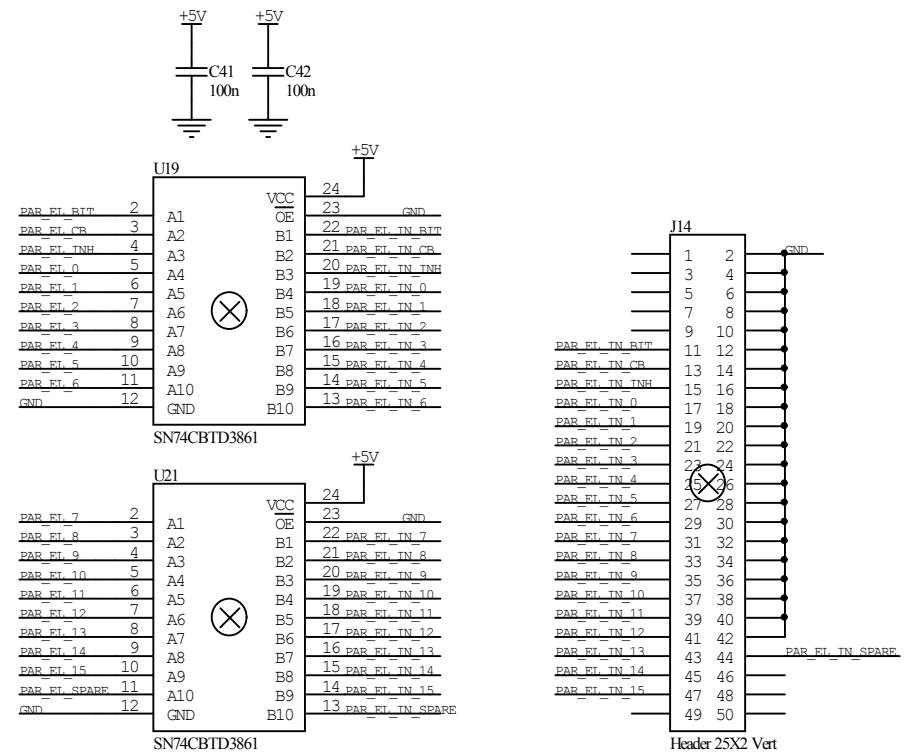
Fiber Optic Angle Link

Title Pedestal Interface - Receiver Link			CSU-CHILL 30750 Weld County Road 45 Greeley, CO 80631	Engineer: JG
Size: Letter	Number: wibex_pi_5	Revision: 1.0	Colorado State University Drawn By: JG	
Date: 3/24/2009	Time: 2:11:25 PM	Sheet 5 of 8		
File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconvert\ac_rxlink.SchDoc				

Parallel Angle Input - Azimuth



Parallel Angle Input - Elevation



Title **Pedestal Interface - Parallel Interface**

CSU-CHILL
30750 Weld County Road 45
Greeley, CO 80631

Engineer:
JG

Size: Letter | Number: wibex_pi_6 | Revision: 1.0

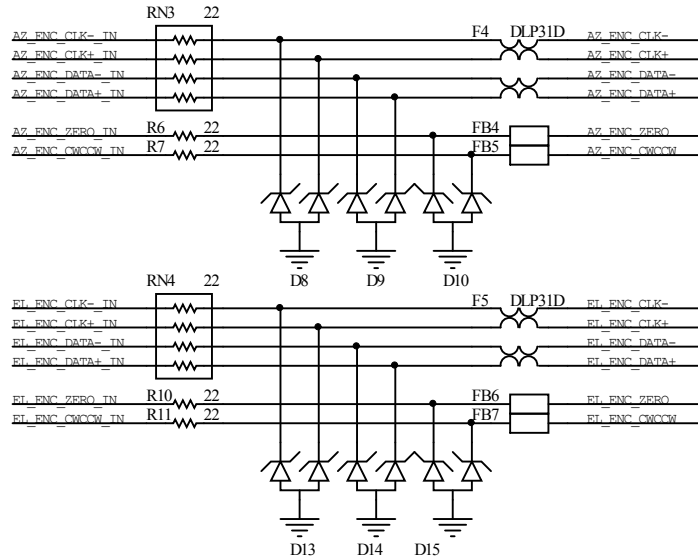
Colorado State University

Drawn By:
JG

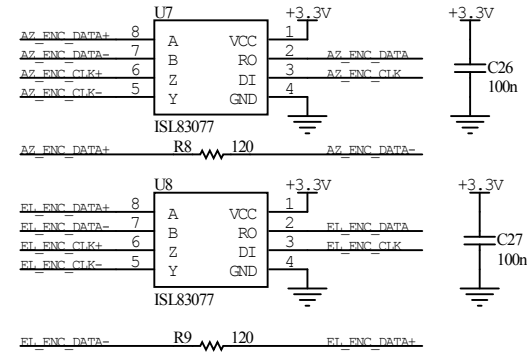
Date: 3/24/2009 | Time: 2:11:25 PM | Sheet 6 of 8

File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconvert\ac_parenc.SchDoc

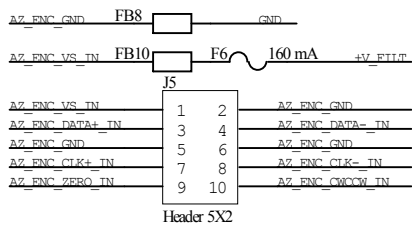
Encoder I/O Protection Network



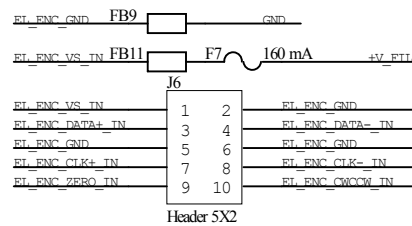
SSI Encoder Driver/Receiver



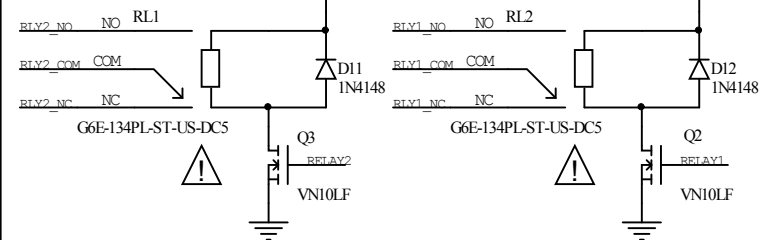
Azimuth Encoder Connector



Elevation Encoder Connector



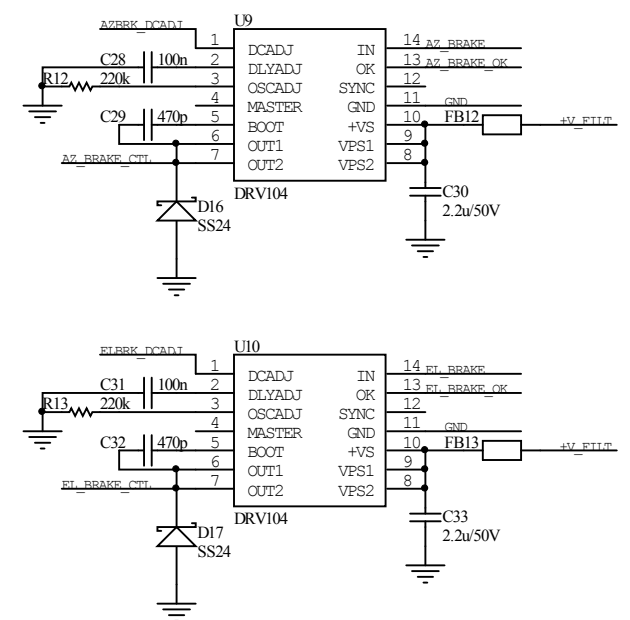
Relay Drivers



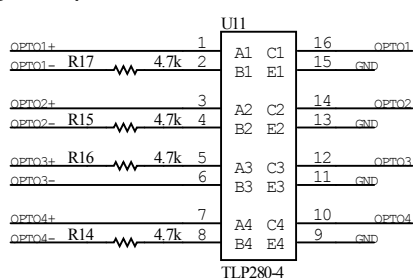
Common I/O, Brake connector



Brake Control



Isolated Digital Inputs



Series resistor values may be changed depending on input voltage range. Optoisolator forward current is 5mA.
 Note: Optoisolators are bidirectional

5V -> 200
 24V -> 4.7k
 120V -> 24k

Title **Pedestal Interface - Encoder Interface**

CSU-CHILL
 30750 Weld County Road 45
 Greeley, CO 80631

Engineer:
 JG

Size: Letter Number: wibex_pi_7 Revision: 1.0

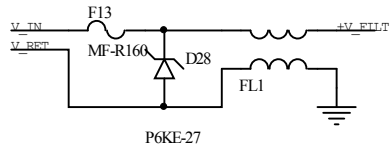
Colorado State University

Drawn By:
 JG

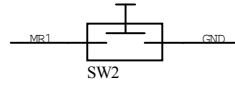
Date: 3/24/2009 Time: 2:11:25 PM Sheet 7 of 8

File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconverter\ac_encoder.SchDoc

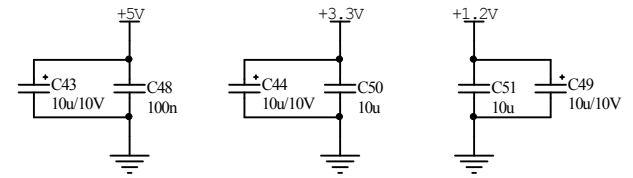
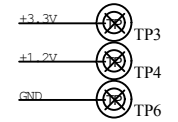
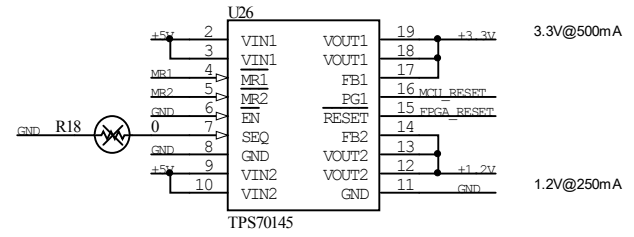
Power Entry, Protection



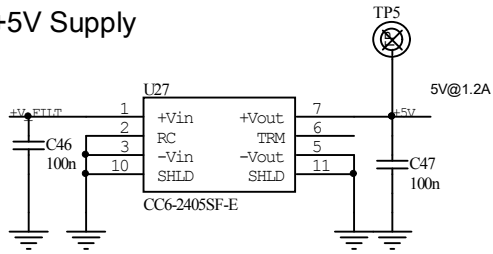
Manual Reset



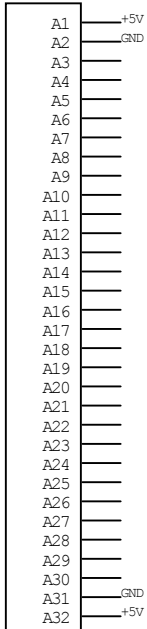
FPGA Supplies



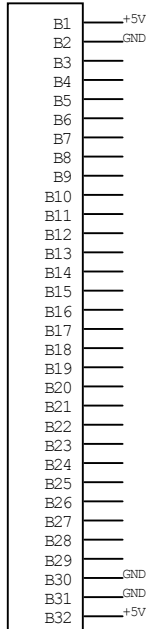
+5V Supply



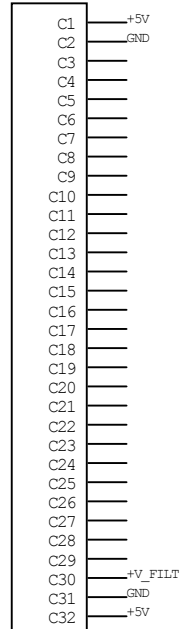
UMAC Chassis connector



P1A



P1B



P1C

Title Pedestal Interface - Power Supplies			CSU-CHILL 30750 Weld County Road 45 Greeley, CO 80631	Engineer: JG
Size: Letter	Number: wibex_pi_8	Revision: 1.0	Colorado State University	
Date: 3/24/2009	Time: 2:11:25 PM	Sheet 8 of 8	Drawn By: JG	
File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconvert\ac_psu.SchDoc				