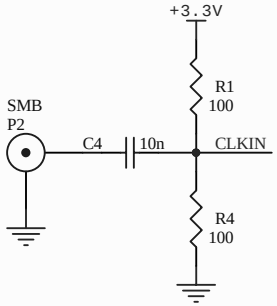
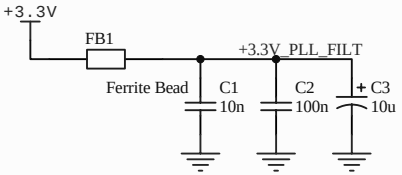
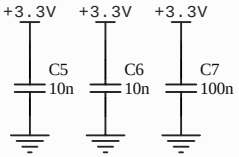
Clock Input

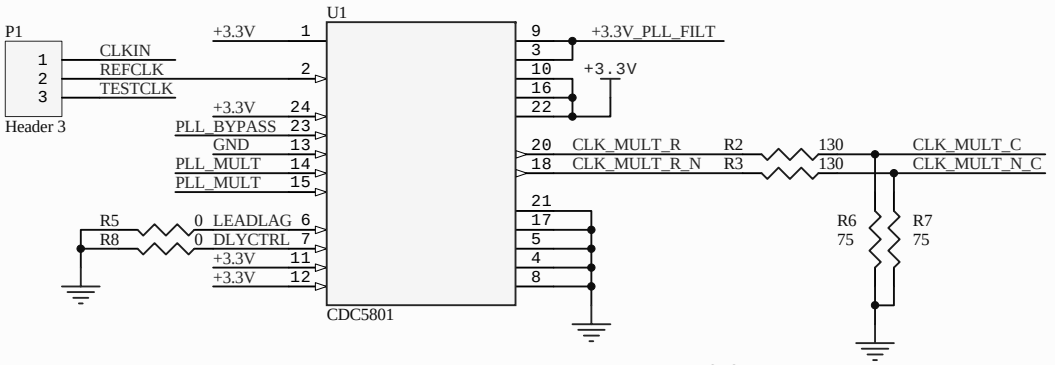


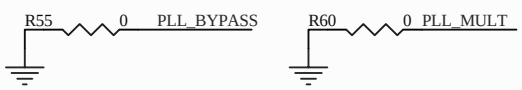
FID?

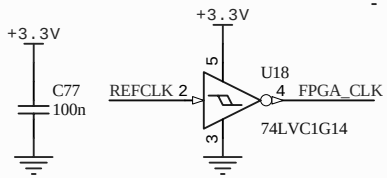
PLL Multiplier



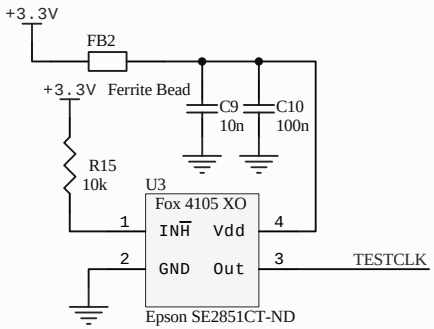




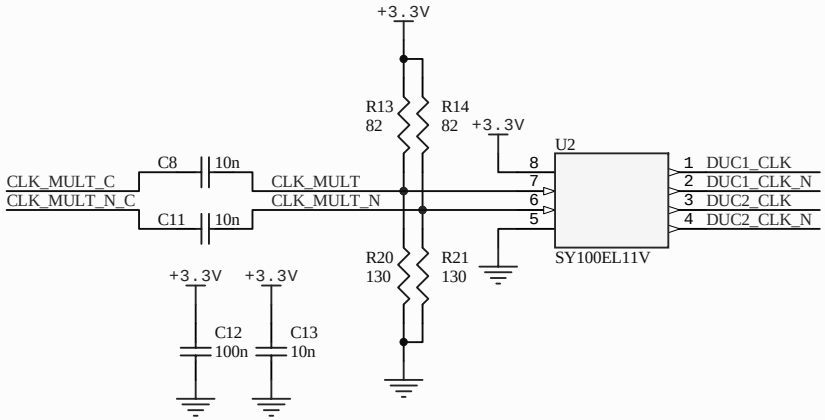


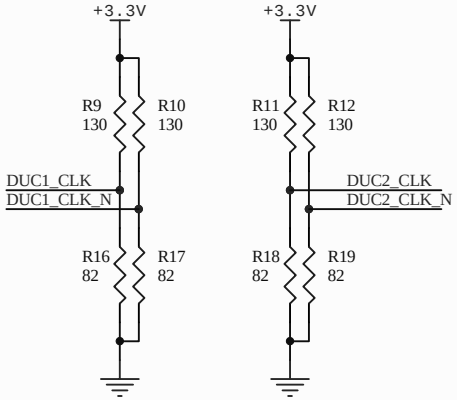


Test Clock Oscillator



Clock Distribution + Termination Network for DUCs

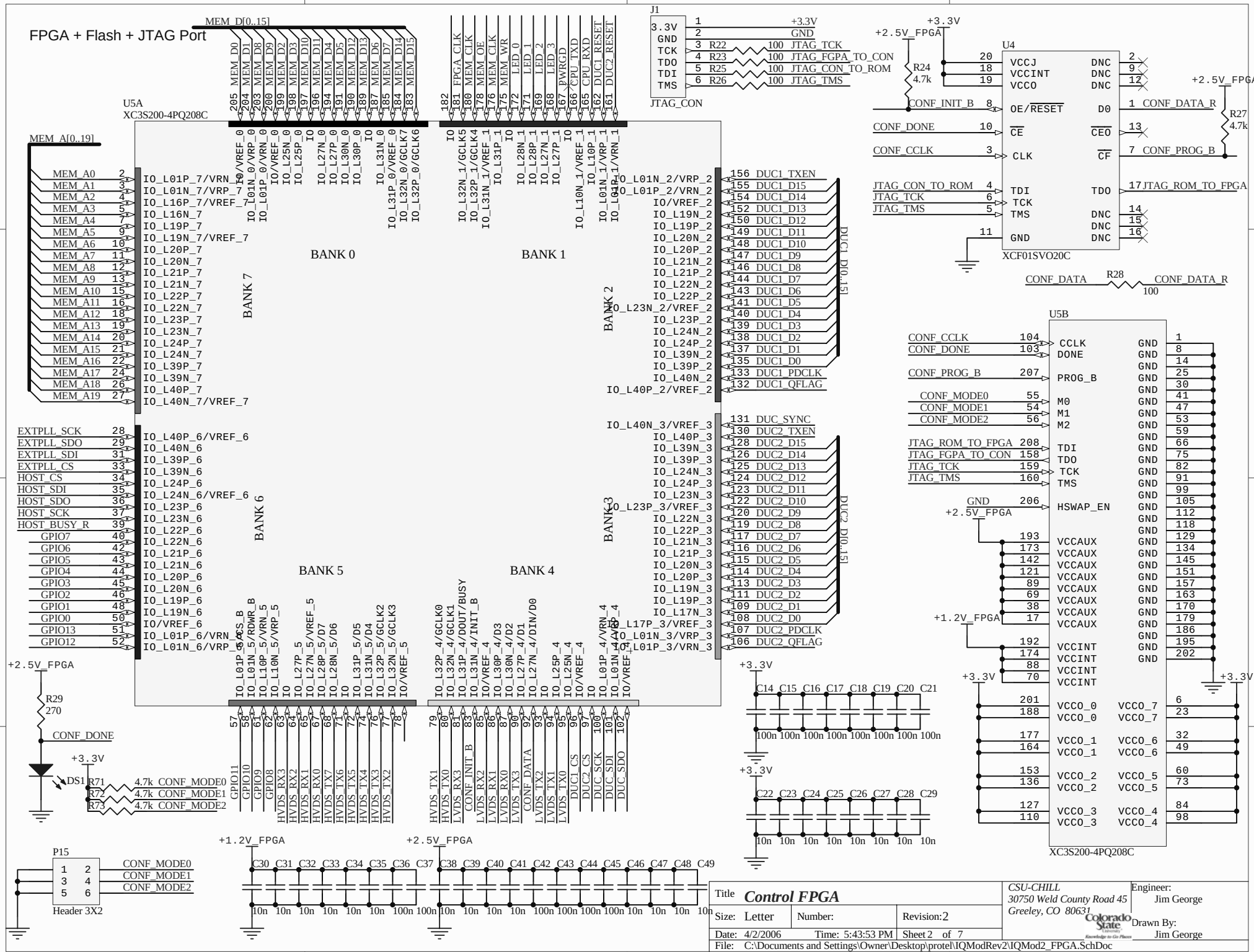




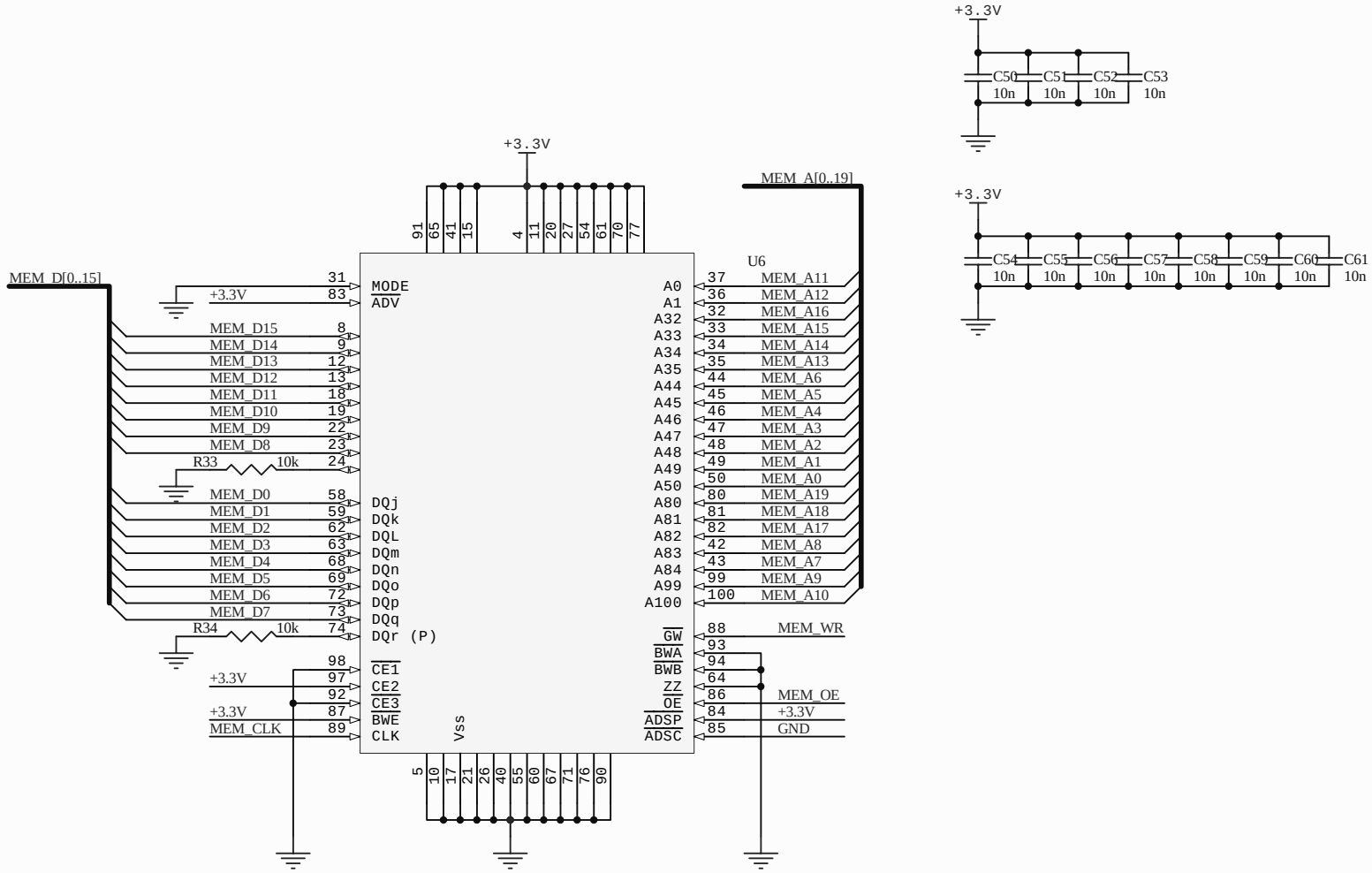
Title	***Clock Source***		
Size: Letter	Number:	Revision: 2	
Date: 4/2/2006	Time: 5:43:53 PM	Sheet 1 of 7	
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_ClkGen.SchDoc			

CSU-CHILL
30750 Weld County Road 45
Greeley, CO 80631
Colorado State University
Knowledge to Go Places

Engineer: Jim George
Drawn By: Jim George


FPGA + Flash + JTAG Port
U5A
XC3S200-4PQ208C
BANK 0
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7
MEM_D[0..15]
MEM_A[0..19]
J1
JTAG_CON
U4
XCF01SVO20C
U5B
XC3S200-4PQ208C
P15
Header 3X2
Title
Control FPGA
Size: Letter
Number:
Revision: 2
Date: 4/2/2006
Time: 5:43:53 PM
Sheet 2 of 7
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_FPGA.SchDoc
CSU-CHILL
30750 Weld County Road 45
Greeley, CO 80631
Engineer: Jim George
Drawn By: Jim George

Memory



Title ***Memory***			*CSU-CHILL* *30750 Weld County Road 45* *Greeley, CO 80631* Colorado State University Knowledge to Go Places
Size: Letter	Number:	Revision: 2	Engineer: Jim George
Date: 4/2/2006	Time: 5:43:54 PM	Sheet 3 of 7	Drawn By: Jim George
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_Memory.SchDoc			

Clock Termination

DUC1_CLK1 — R61 100 — DUC1_CLK1C

DUC1_CLK — C138 100n — DUC1_CLK2

DUC1_CLK_N — C139 100n — DUC1_CLK2C

Mounted for PLL-Clock Only

DUC1_CLK2 — R62 100 — DUC1_CLK2C

DUC1_CLK — C140 100n — DUC1_CLK1

DUC1_CLK_N — C141 100n — DUC1_CLK1C

Data Termination

RN5 (22)

DUC1_D11	DUC1_D11_R
DUC1_D10	DUC1_D10_R
DUC1_D9	DUC1_D9_R
DUC1_D8	DUC1_D8_R

RN6 (22)

DUC1_D15	DUC1_D15_R
DUC1_D14	DUC1_D14_R
DUC1_D13	DUC1_D13_R
DUC1_D12	DUC1_D12_R

RN7 (22)

DUC1_D3	DUC1_D3_R
DUC1_D2	DUC1_D2_R
DUC1_D1	DUC1_D1_R
DUC1_D0	DUC1_D0_R

RN8 (22)

DUC1_D7	DUC1_D7_R
DUC1_D6	DUC1_D6_R
DUC1_D5	DUC1_D5_R
DUC1_D4	DUC1_D4_R

DUC Power

U17B

+3.3V_DUC1: 1, 4, 7, 9, 12, 17, 19, 22, 25

+1.8V_DUC1: 27, 38, 45, 57, 69, 81, 88, 93, 99

+3.3V_IOVDD1: 47, 79

+3.3V_PLL1: 65

+3.3V_CLK1: 58, 64

+3.3V_DUC1: 2, 3, 8, 10, 14, 16, 18, 23, 24

+1.8V_DUC1: 26, 32, 37, 44, 56, 68, 82, 89, 100

+3.3V_IOVDD1: 46, 80

+3.3V_PLL1: 67

+3.3V_CLK1: 61

+1.8V_DUC1 — R70 10 — +1.8V_DUC1

C145 10n

Digital Upconverter

U17A

DUC1_CLK1	59	92	
DUC1_CLK1C	60	91	
DUC1_CLK2	62	90	
DUC1_CLK2C	63	87	
DUC1_RESET	95	86	
DUC1_D15_R	34	85	
DUC1_D14_R	35	84	
DUC1_D13_R	36	83	
DUC1_D12_R	39	78	
DUC1_D11_R	40	77	
DUC1_D10_R	41	76	
DUC1_D9_R	42	75	
DUC1_D8_R	43	74	
DUC1_D7_R	48	73	
DUC1_D6_R	49	72	
DUC1_D5_R	50	71	
DUC1_D4_R	51		
DUC1_D3_R	52		
DUC1_D2_R	53		
DUC1_D1_R	54		
DUC1_D0_R	55		
DUC_SYNC	94	21	
DUC1_PDCLK	70	20	
DUC1_QFLAG	98	5 IOUT1	
DUC1_TXEN	33	6 IOUT1C	
DUC_SCK	29	66 PLL_FILT1	
DUC1_CS	28	13 BIAS1	
DUC_SDI	30	15	
DUC_SDO	31	11 BFLT1	
GND	97		
GND	96		

EXTLO

+3.3V_DUC1

R64 50 — R65 50

R67 100

T2 — T1-1T — IFOUT1 — P13

1:1 RF Transformer

R68 63.4

R69 1k

C142 330p

C144 33n

C143 100n

Mount only if PLL is enabled

R(BIAS)

$$IOUT(FS) = \frac{16 \times V(EXTIO)}{R(BIAS)}$$

V(EXTIO)=1.2V

+3.3V_DUC1: C146 C147 C148 C149 C150 C151 C152 C153 C154 C155 — 100n 100n 100n 100n 100n 100n 100n 100n 100n 10u

+1.8V_DUC1: C156 C157 C158 C159 C160 C161 C162 C163 C164 — 100n 100n 100n 100n 100n 100n 100n 100n 100n 22u

+3.3V_IOVDD1: C166 C167 C168 C169 — 100n 100n 10u 10u

+3.3V_CLK1: C170 — 100n

+3.3V_PLL1 — C165 10n

Mount 0-ohm resistor to disable PLL

Title	**Digital Upconverter, CH1**		
Size: Letter	Number:	Revision: 2	
Date: 4/2/2006	Time: 5:43:54 PM	Sheet 4 of 7	
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_DUC1.SchDoc			

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30750 Weld County Road 45
Greeley, CO 80631
Colorado State University

Engineer: Jim George
Drawn By: Jim George

Clock Termination

DUC2_CLK1 — R50 100 — DUC2_CLK1C

DUC2_CLK — C104 100n — DUC2_CLK2

DUC2_CLK_N — C105 100n — DUC2_CLK2C

Mounted for PLL-Clock Only

DUC2_CLK2 — R51 100 — DUC2_CLK2C

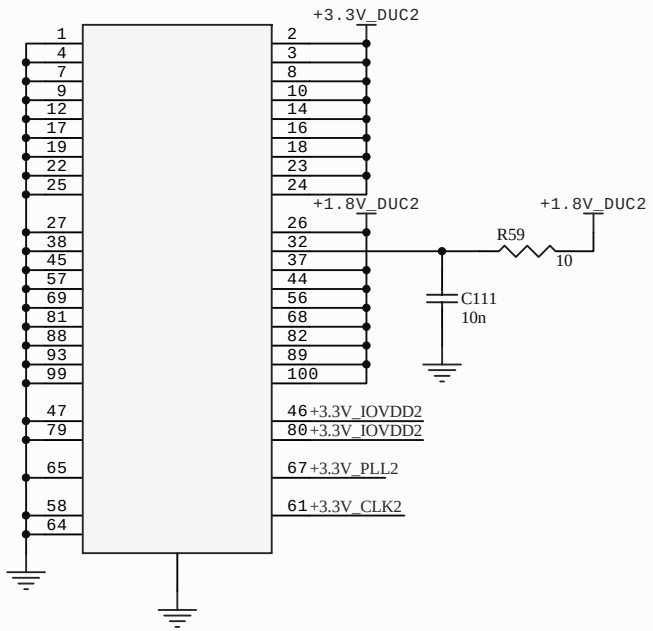
DUC2_CLK — C106 100n — DUC2_CLK1

DUC2_CLK_N — C107 100n — DUC2_CLK1C

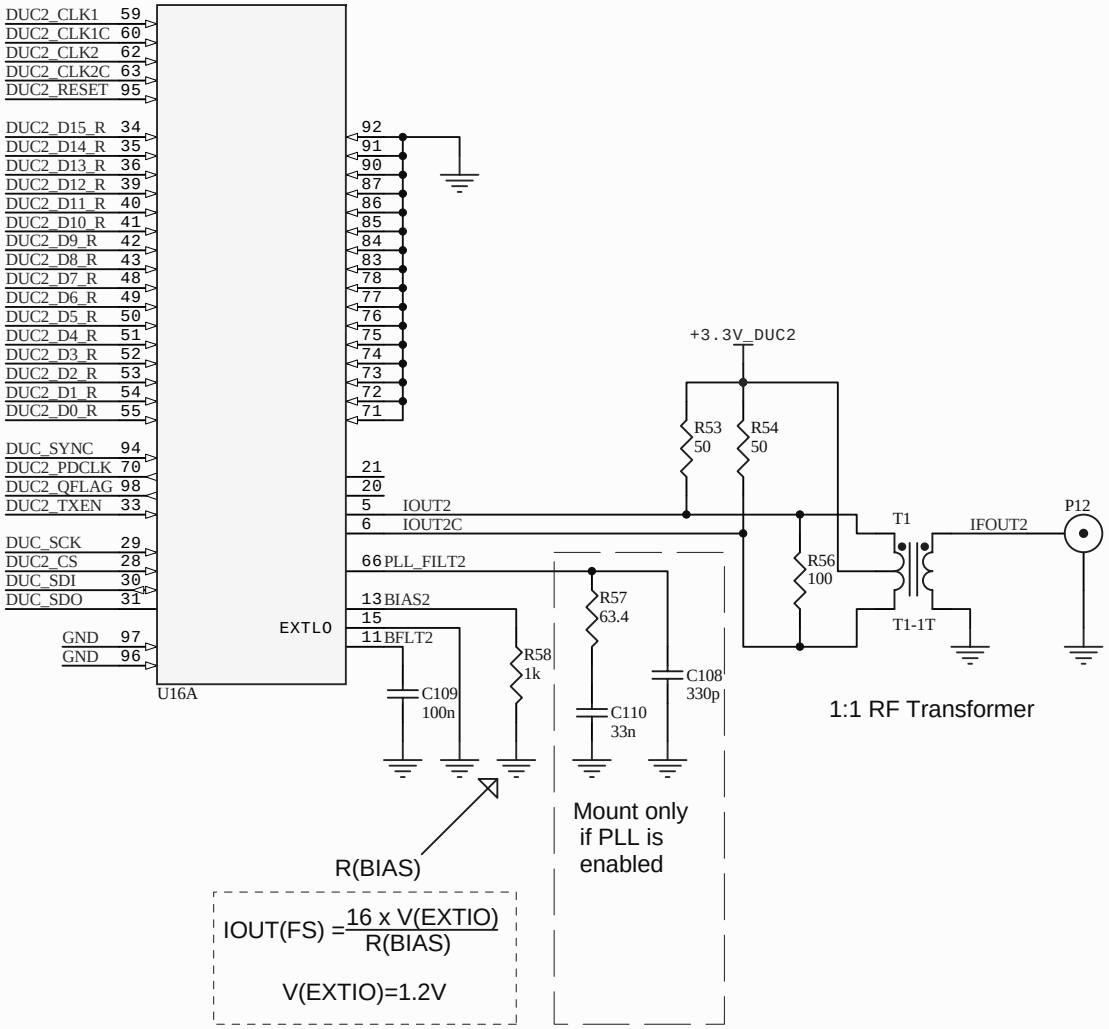
Data Termination

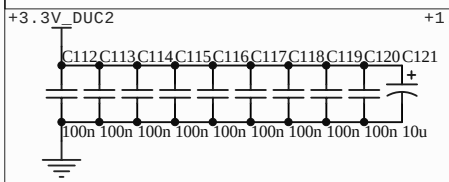
DUC2_D11	RN1	DUC2_D11_R	DUC2_D15	RN2	DUC2_D15_R
DUC2_D10		DUC2_D10_R	DUC2_D14		DUC2_D14_R
DUC2_D9		DUC2_D9_R	DUC2_D13		DUC2_D13_R
DUC2_D8	22	DUC2_D8_R	DUC2_D12	22	DUC2_D12_R
DUC2_D3	RN3	DUC2_D3_R	DUC2_D7	RN4	DUC2_D7_R
DUC2_D2		DUC2_D2_R	DUC2_D6		DUC2_D6_R
DUC2_D1		DUC2_D1_R	DUC2_D5		DUC2_D5_R
DUC2_D0	22	DUC2_D0_R	DUC2_D4	22	DUC2_D4_R

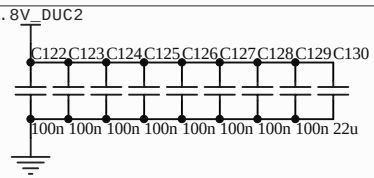
DUC Power

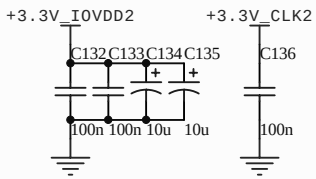


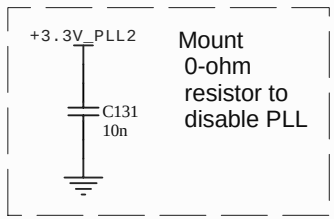
Digital Upconverter





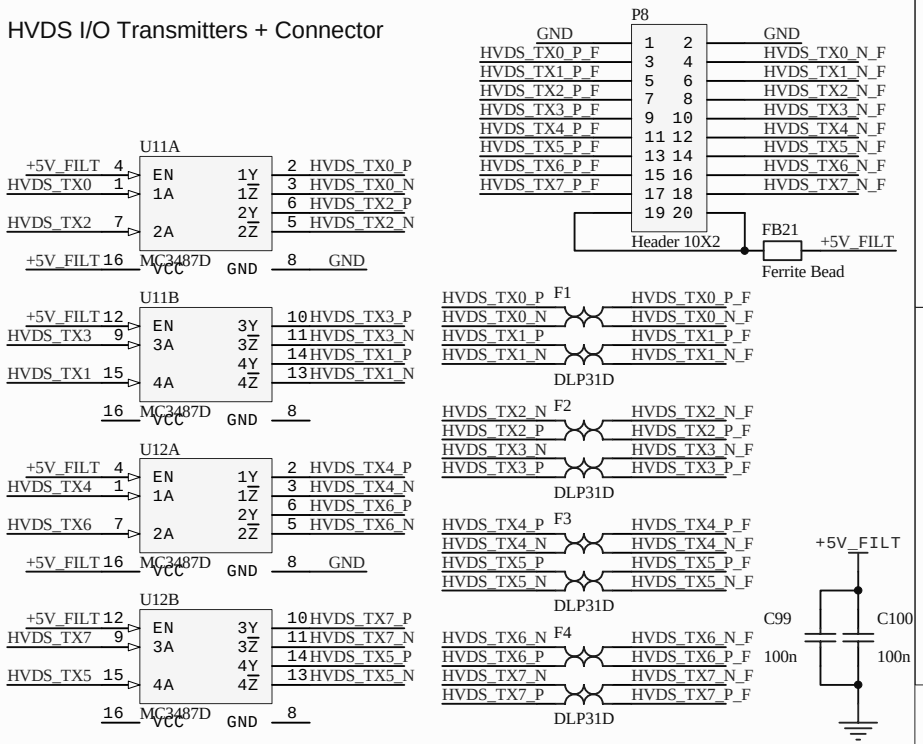




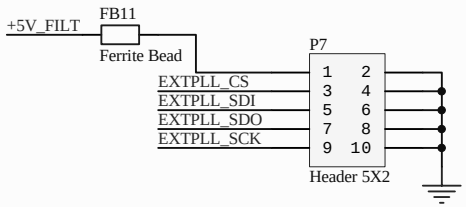


Title: ***Digital Upconverter, CH2***			*CSU-CHILL* *30750 Weld County Road 45* *Greeley, CO 80631* Engineer: Jim George
Size: Letter	Number:	Revision: 2	Drawn By: Jim George
Date: 4/2/2006	Time: 5:43:54 PM	Sheet 5 of 7	
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_DUC2.SchDoc			

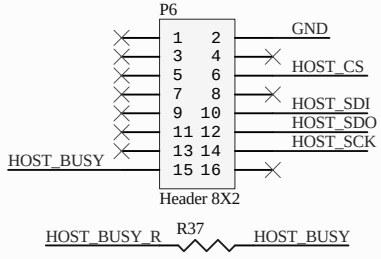
HVDS I/O Transmitters + Connector



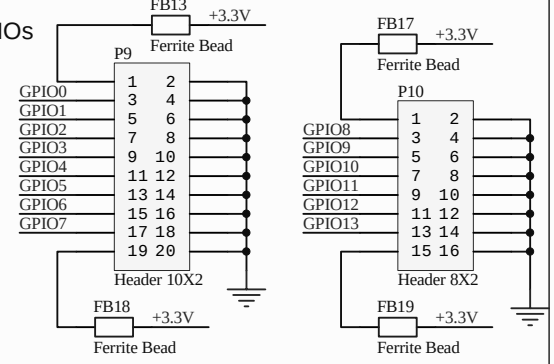
External RF PLL Interface



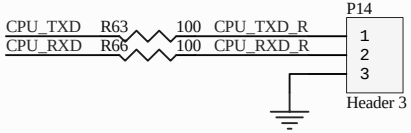
Host Interface



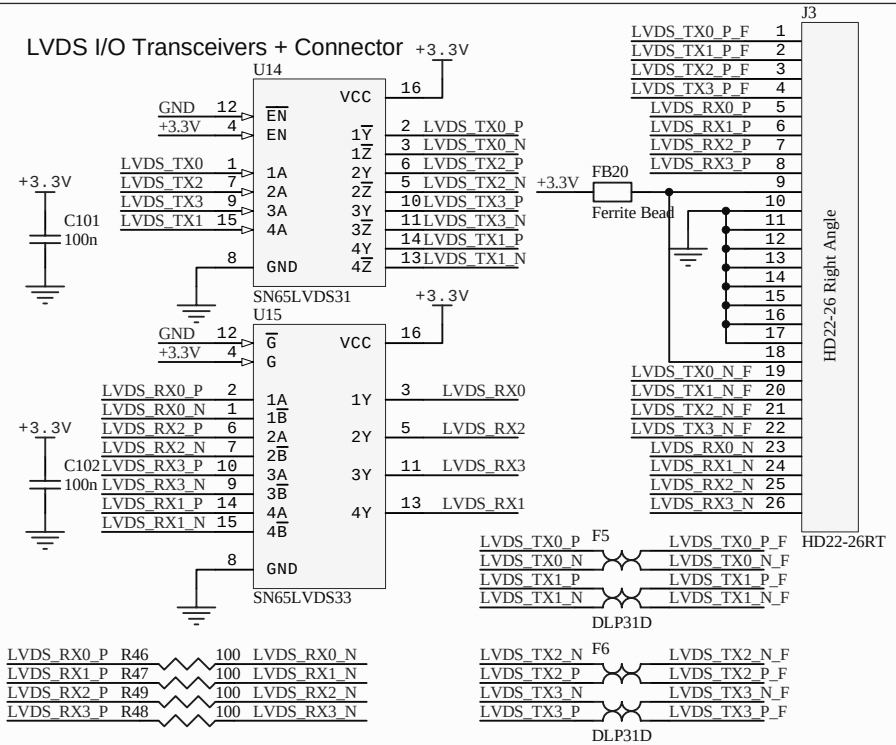
GPIOs



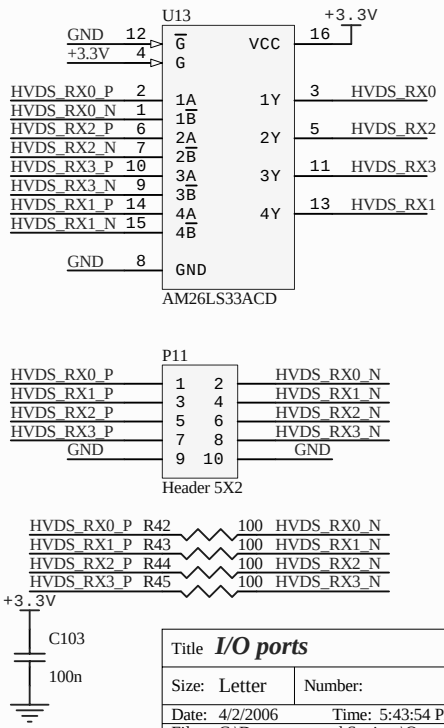
Picoblaze RS-232



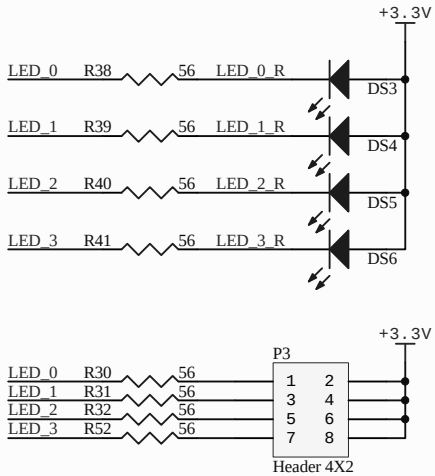
LVDS I/O Transceivers + Connector



HVDS I/O Receivers + Connector



LEDs



Title	***I/O ports***		
Size: Letter	Number:	Revision: 2	
Date: 4/2/2006	Time: 5:43:54 PM	Sheet 6 of 7	
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_IO.SchDoc			

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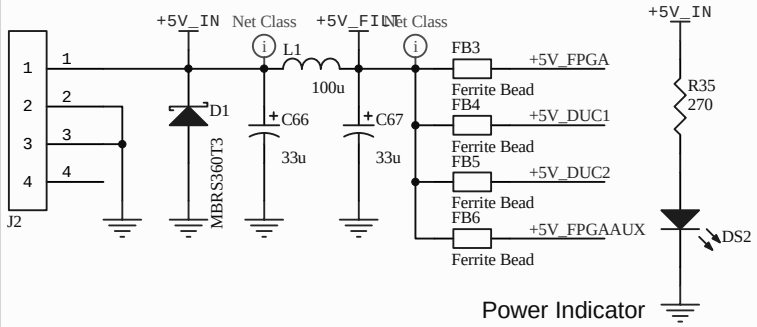
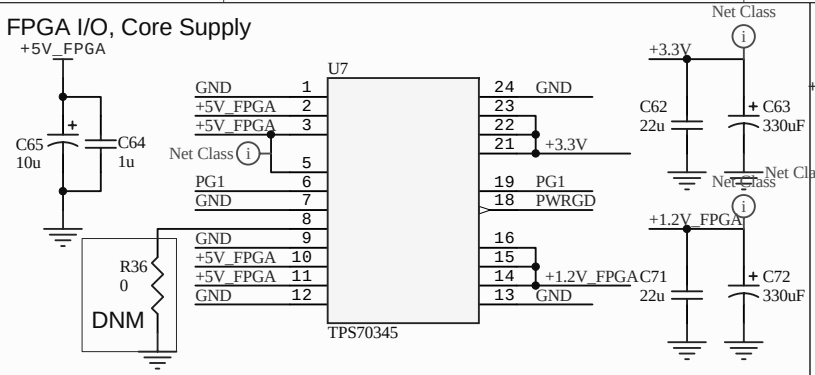
30750 Weld County Road 45
Greeley, CO 80631
Colorado State University
Engineer: Jim George
Drawn By: Jim George

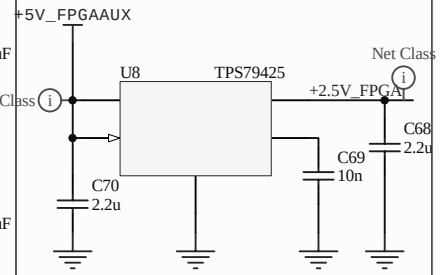
Input Connector + pi-Filter



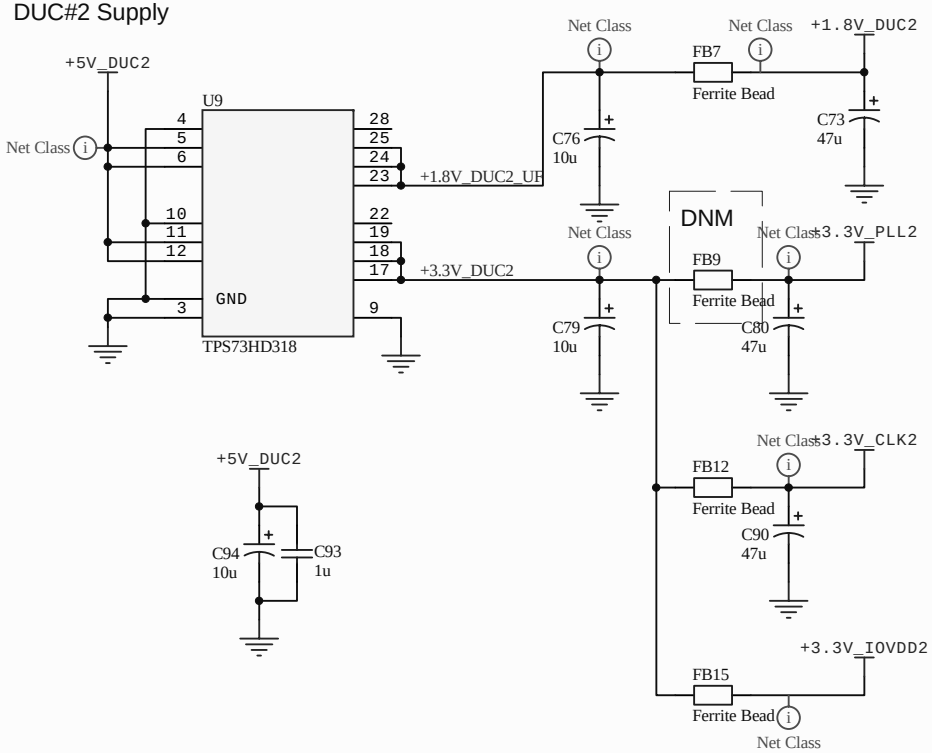
FPGA I/O, Core Supply



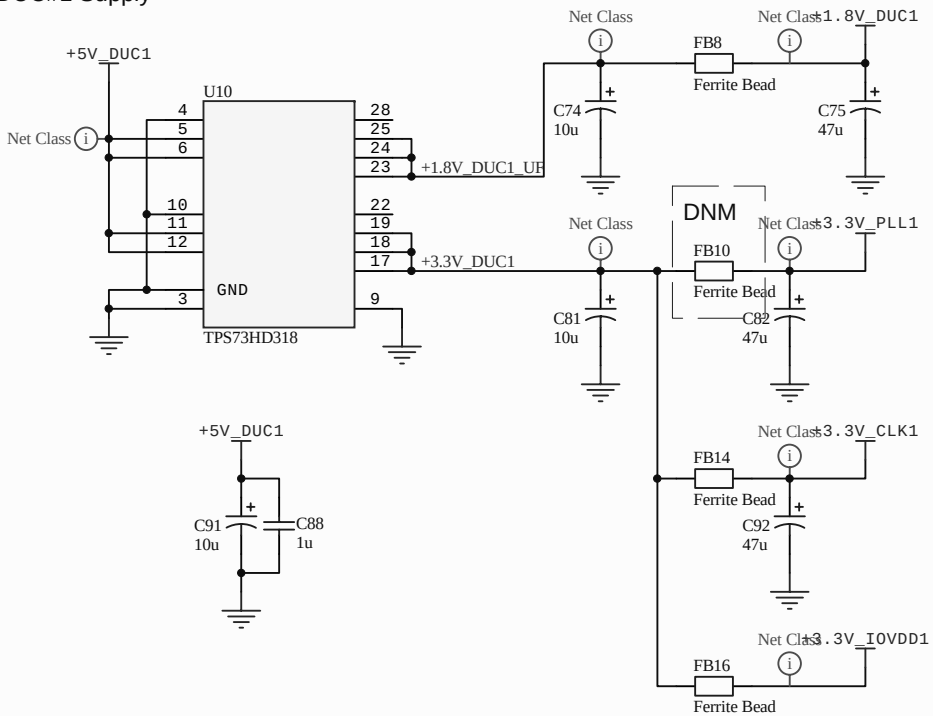
FPGA Auxiliary Supply



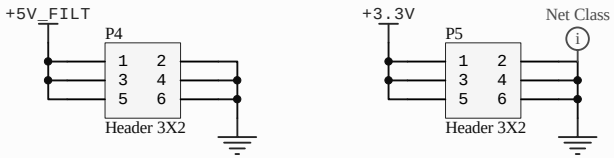
DUC#2 Supply



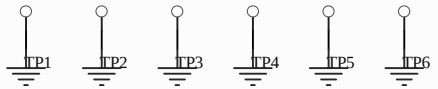
DUC#1 Supply



External Power



Ground Testpoints



Title	***Power Supply***		
Size: Letter	Number:	Revision: 2	
Date: 4/2/2006	Time: 5:43:55 PM	Sheet 7 of 7	
File: C:\Documents and Settings\Owner\Desktop\protel\IQModRev2\IQMod2_PSU.SchDoc			

CSU-CHILL
30750 Weld County Road 45
Greeley, CO 80631

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Drawn By: Jim George